Introduction To VLSI Design

Spring 2016

Homework #1

Due Date: Thursday (03/17/2016)

N.B. Submit detailed calculation and appropriate figures when needed.

1. Solve the following problems for a CMOS inverter

Given: and

and

and

and

1. Find the propagation delay. (2.5)
2. Find the rise time and fall time. (2.5)
3. Find the maximum obtainable (theoretical) frequency. (2.5)
4. Is the inverter symmetrical, if not how to make it a symmetrical inverter? (2.5)
5. An NMOS transistor has the following parameters

If , then

1. In what region the NMOS transistor is operating? (2.5)
2. Find the drain current at this operating region. (2.5)
3. If all other voltages remain unchanged only VDS is allowed to change what is the highest value of VDS when the given transistor will be in linear region? (5)
4. With the given parameters and the applied voltages will there be a uniform channel between the source and drain of the transistor? Why and why not (give your answer in maximum two lines). (2.5)
5. What will be effect on current (ID) of the transistor if you change the width of the transistor to 2W and the length to 0.25L? (5)
6. How oxide thickness (tox) affects the current? (2.5)
7. Solve the following problems for a CMOS inverter

Given: and

and

Both NMOS and PMOS have equal channel length

1. Find for . (5)
2. Find for making the inverter symmetrical. (5)
3. If , then what will be the value of the switching threshold voltage? (5)
4. Keeping all the dimensions unchanged if the thickness () of both NMOS and PMOS are increased to what will be the value of . (5)
5. For a static CMOS the following parameters are given

and

and

and

Find the following

1. Output high and low voltages () (4)
2. Input high and low voltages () (16)
3. Inverter switching threshold voltage (8)
4. Condition for the inverter to be symmetrical (4)
5. Logic swing and transition width (4)
6. Noise margin () (4)
7. For an Pseudo NMOS inverter (Gate is grounded for PMOS and Input is applied in the gate terminal of NMOS) find the following:

and

and

and

1. Output high and low voltages () (5)
2. Input high and low voltages () (5)
3. Inverter switching threshold voltage (5)
4. Noise margin () (5)
5. Consider a 4-input NOR function with inputs A, B, C and D
6. Draw the circuit of that NOR gate using CMOS logic principle where A is the most active and B is the least active input. (5)
7. Consider that the worst-case propagation delay for the circuit is 500ns. If you use uniform sizing for the transistor in the critical path (the path corresponds to the worst-case delay) what will be the sizes of the transistors for the logic gate to be symmetrical (equal worst-case and ). (15)

Note: and . Consider the load capacitance (CL) of the logic gate is 500pF and every internal circuit node in the circuit has an internal node capacitance of 100pF. The resistance of a unit size NMOS transistor is Rno=20kΩ and the resistance of a unit size PMOS transistor is Rpo=60kΩ.

Hint: Use Elmore-delay model to calculate the sizes of the transistors.

1. In a fabrication process the wafer diameter is 30cm. the technology parameter α = 2.0. the number of defects per cm2 is 1. Calculate
2. How many dies can be obtained if the area of each die is 600 mm2? (5)
3. What percentage (yield) of the obtained dies will be functional? (5)
4. A logic function is given below:

Implement the above logic function using the following circuit style

1. Static CMOS (5)
2. depletion load NMOS (5)
3. pseudo-NMOS (5)
4. Dynamic CMOS (5)
5. Implement the following logic function using Differential Cascode Voltage Switch Logic (DCVSL) (10)